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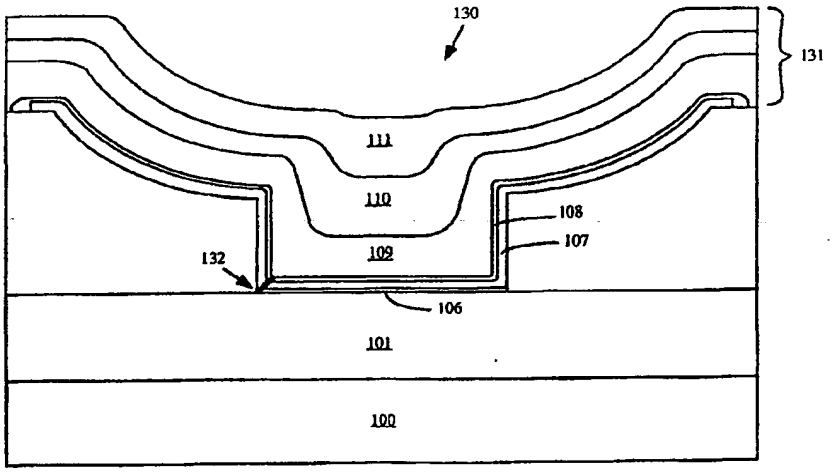

(57) Abstract

An antifuse is provided which includes a first conductive layer (101), an antifuse layer (106, 107, 108) formed on the first conductive layer, and a second conductive layer (109) formed on the antifuse layer. A portion of the antifuse layer forms a substantially orthogonal angle with the first conductive layer and the second conductive layer. This "corner" formation of the antifuse enhances the electric field at this location during programming, thereby providing a predictable location for the filament, i.e. the conductive path between the first and second conductive layers. This antifuse provides other advantages including: a relatively low programming voltage, good step coverage for the antifuse layer and the upper conductive layer, a low, stable resistance value, and minimal shearing effects on the filament.

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ANTIFUSE STRUCTURE WITH INCREASED BREAKDOWN AT EDGES

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of U.S. Patent Application Serial No. 07/933,428, entitled "Antifuse Structure and Method for Forming", filed August 21, 1992 (Atty.Doc.No. M-2164).

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to antifuses, and in particular to an antifuse structure with an increased breakdown at the edges of an antifuse layer.

Description of the Related Art

Antifuses are well known in the art. An antifuse is a structure which is non-conductive when manufactured, but becomes permanently conductive by applying a predetermined voltage across its terminals. Antifuses are typically used in programmable logic devices to programmably interconnect conductive lines.

Figures 1A-1D illustrate a conventional method of forming an antifuse. Referring to Figure 1A, a polycrystalline silicon layer 11 is formed on substrate 10 to provide a lower conductive terminal for the antifuse. An insulation layer 13 is then deposited and patterned to partially expose polycrystalline silicon layer 11 as shown in Figure 1B. Referring to Figure 1C, an amorphous silicon layer 14 is then deposited and patterned to cover the exposed portion of polycrystalline silicon layer 11 and portions of insulation layer 13 adjacent to polycrystalline silicon layer 11. Referring to Figure 1D, conductive layers 18, including titanium layer 15, titanium nitride layer 16, and aluminum-silicon layer 17, are formed over amorphous silicon layer 14, and then patterned (not shown) to form an upper conductive terminal.

However, antifuse 20 requires a relatively high voltage, typically 12-14 volts, to program. Standard transistors used in 5-volt integrated circuit systems typically break down between 12-14 volts. Thus, special processing is needed to enhance the breakdown characteristic of the transistors for programming the antifuse. Moreover, to ensure proper operation of the integrated circuit system, other structures in the system must be isolated from the antifuse programming voltages.

Furthermore, antifuse 20 is undesirably affected by internal temperatures generated during programming. Specifically, during programming of antifuse 20, the leakage current of this device increases with the increase in applied voltage. Eventually, the leakage current focuses on a localized weak spot in amorphous silicon layer 14. A thermal runaway condition then develops which results in localized heating and, eventually, filament formation between the upper conductive terminal and the lower conductive terminal. The different thermal expansion coefficients of the materials in different layers of the antifuse structure in turn cause stresses to develop in the material as it cools after programming. Over time, these stresses will relax, producing movement between layers of the antifuse material.

Figure 2A shows a partial top view of antifuse 20 after programming in which filament 19 joins titanium layer 15 (Figure 1D) and polysilicon layer 11. Note that Figure 2A illustrates an edge 21 of amorphous silicon layer 14 that contacts polycrystalline silicon layer 11. As described above, stress relaxation occurs within amorphous silicon layer 14, not at its boundaries. Therefore, referring to Figure 2B, if shearing occurs in prior art antifuse 20 due to stress relaxation, the sheared portion 19' of filament 19 significantly reduces the surface area 19A for conducting current, thereby resulting in instability of the resistance provided by antifuse 20.

Therefore, a need arises for an antifuse which programs at a relatively low programming voltage and ensures a stable resistance irrespective of shearing conditions.

SUMMARY OF THE INVENTION

In accordance with the present invention, an antifuse comprises a first conductive layer, an antifuse layer formed on the first conductive layer, and a second conductive layer formed on the antifuse layer. A portion of the antifuse layer forms a substantially orthogonal angle with the first conductive layer and again with the second conductive layer. This "double corner" formation of the antifuse layer enhances the electric field during programming. Thus, the resulting filament, i.e. the conductive path between the first and second conductive layers formed during programming, consistently forms along this corner.

The present invention provides advantages under shearing conditions due to stress relaxation that typically occur within the programmed antifuse structure. Specifically, because a filament in accordance with the present invention is formed at one of the boundaries of the antifuse, not within the antifuse structure, the filament is substantially unaffected by shearing conditions caused by stress relaxation. Therefore, an antifuse in accordance with the present invention provides a stable resistance even under stress relaxation conditions.

Furthermore, in contrast to the prior art antifuses which have a programming voltage of 12-14 volts, an antifuse in accordance with the present invention has a programming voltage of 8-9 volts. Thus, ordinary transistors which break down at 12-14 volts can be used both for programming antifuses and for logic functions.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1D illustrate one method of forming a conventional antifuse.

Figure 2A shows a partial view of the conventional antifuse illustrated in Figure 1D after programming.

Figure 2B shows a partial view of the conventional antifuse illustrated in Figure 1D after shearing occurs.

Figures 3A-3J illustrate one method of forming an antifuse in accordance with the present invention.

Figure 4 shows a partial view of the antifuse illustrated in Figure 3J after programming.

DETAILED DESCRIPTION OF THE DRAWINGS

Figures 3A-3J illustrate the steps to provide one embodiment of an antifuse in accordance with the present invention. Referring to Figure 3A, a conductive layer 101, approximately 4500Å to 7000Å thick, is formed on substrate 100. In this embodiment of the present invention, conductive layer 101 includes two layers, bottom layer 101A and top layer 101B. The bottom layer 101A is aluminum (Al) having a thickness of approximately 3500Å to 6500Å. The top layer 101B is titanium-tungsten (TiW) having a thickness of approximately 1000Å to 3000Å. Layer 101B is formed on top of layer 101A to prevent the diffusion of aluminum into a to-be-formed amorphous silicon layer (shown in Figure 3H). In other embodiments, bottom layer 101A is aluminum-silicon (AlSi) or aluminum-silicon-copper (AlSiCu) and top layer 101B is titanium-nitride (TiN). In yet other embodiments of the present invention, conductive layer 101 is formed solely from titanium-tungsten (TiW). Conductive layer 101 forms the lower conductive terminal (hereinafter lower conductive terminal 101) of the to-be-formed antifuse.

After formation of this lower conductive terminal, a layer of undoped oxide, for example silicon dioxide, is deposited at a temperature of about 400°C to a thickness of approximately 15,000Å. This oxide serves as a sacrificial oxide during the subsequent planarization process. Specifically, as shown in Figure 3A, a photoresist layer 102A is deposited on layer 102. Then, an etch removes

photoresist layer 102A and approximately 9,000Å to 11,000Å of oxide layer 102.

As is well known in the art, photoresist layer 102A forms a planar surface on the somewhat irregular surface of oxide layer 102. Etching of thinner portions of photoresist occurs more rapidly than thicker portions of photoresist. Thus, after removal of photoresist layer 102A and a portion of oxide layer 102, a substantially planar surface is provided on oxide layer 102 as shown in Figure 3B.

Referring to Figure 3C, after the oxide etch, another oxide layer 103, approximately 8000Å thick, is deposited at a temperature of about 400°C to a thickness between 9,000Å and 10,000Å on oxide layer 102 to ensure adequate isolation between lower conductive terminal 101 and the to-be-formed upper conductive terminal.

Then, a photoresist layer 104 is deposited and patterned as shown in Figure 3D. A subsequent isotropic etch forms the opening 105A which is shown in Figure 3E. Typically, this isotropic etch uses a conventional, diluted HF solution which etches down approximately 5500Å to 7500Å. In one embodiment of the present invention, the HF solution etches down 6500Å. In other embodiments, other etching processes, such as a plasma etch, are used to provide the angle 140, typically 40 degrees, which is measured from the beginning of the slope (point 140A) to the end of the slope (point 140B). This angle ensures good step coverage of the to-be-formed antifuse layer and the upper conductive layer in opening 105A.

Referring to Figure 3F, an anisotropic etch removes a portion of oxide layer 103 and oxide layer 102, thereby exposing lower conductive terminal 101. In this embodiment, the anisotropic etch is a plasma etch including a mixture of Freon-23 (CHF_3) and oxygen (O_2) at approximately 25°C. This anisotropic etch provides the via 105B.

Subsequent to via definition, an oxygen plasma treatment is performed. During this oxygen plasma treatment, the temperature of the antifuse structure rises

from approximately 25°C to approximately 125°C. The combination of elevated temperature and reactive oxygen plasma produces an oxide layer 106 on lower conductive terminal 101 in via 105B as shown in Figure 3G. Oxide layer 106 is typically an oxide of the material of lower conductive terminal 101. Thus, oxide layer 106 is either titanium oxide, tungsten oxide, or a mixture of titanium oxide and tungsten oxide. In this embodiment, oxide layer 106 is between 35Å and 70Å thick.

Then, referring to Figure 3H, an amorphous silicon layer 107 is deposited in via 105B as well as areas adjacent to via 105B. Amorphous silicon layer 107 is typically deposited to a thickness of between 350Å and 550Å to ensure that this deposition follows the contour of via 105B. In one embodiment of the present invention, amorphous silicon layer 107 is 450Å thick and is formed by using pure silane gas (SiH_4) at a temperature of 300°C and a pressure of 250 mTorr. In another embodiment, a mixture of silane gas and nitrogen (N_2) at a temperature of 300°C is used to produce amorphous silicon layer 107. In that embodiment, amorphous silicon layer 107 has a typical nitrogen content (measured by number of atoms) of between 10% to 20%.

To improve the amorphous nature of amorphous silicon layer 107, i.e. break up any small crystals and reduce leakage, an argon implant, not shown, is performed at a dosage of $1x10^{16}$ atoms/cc and an energy of 30 keV. Other implant dopants such as silicon, oxygen, or arsenic are alternatively used in other embodiments. Then, a photoresist layer (not shown) is deposited and patterned to define the edge 107A of the antifuse. An anisotropic etch etches the exposed portions of amorphous silicon layer 107, thereby providing the edges 107A shown in Figure 3H. Subsequent to this anisotropic etch, another oxygen plasma treatment is performed, thereby forming a silicon dioxide layer 108 approximately 10-30Å thick which covers amorphous silicon layer 107 as shown in Figure 3I. Finally, an upper

conductive terminal 131 is formed using conventional methods.

In one embodiment shown in Figure 3J, upper conductive terminal 131 includes a titanium layer 109, a titanium-tungsten layer 110, and an aluminum-silicon-copper alloy layer 111. In other embodiments, upper conductive terminal 131 is formed from consecutive layers of titanium, titanium-nitride, titanium-tungsten, or consecutive layers of aluminum (formed on amorphous silicon layer 107), aluminum-silicon, and aluminum-silicon-copper.

In the embodiment of the present invention shown in Figure 3H, antifuse 130 typically needs a programming voltage between 7.5 and 10 volts to form a conductive filament 132 which connects upper conductive terminal 131 and lower conductive terminal 101. Because standard transistors can withstand this low antifuse programming voltage, transistors in the antifuse structure can be small, density is high, and no special transistor processing steps are needed.

Moreover, a prior art antifuse having a typical length of 1500Å provides an undesirably high resistance value on the order of 150Ω. In contrast, the short length, i.e. approximately 350Å to 550Å, of conductive filament 132 provides a significantly lower resistance value of approximately 50Ω.

Furthermore, a prior art antifuses exhibits an unstable resistance value at stress current close to the programming current. A more detailed explanation of this phenomena is described in an article entited, "Antifuse Structure Comparison for Field Programmable Gate Arrays" by S. Chiang et al., IEEE IDEM, pages 611-614, 1992, which is herein incorporated by reference in its entirety. In contrast, an antifuse in accordance with the present invention provides a stable resistance value both under low current stress and under DC current stress close to the programming current over a time period of more than 1,000 hours.

As described above, the present invention provides that a portion of the composite antifuse layer, i.e. oxide

layer 106, amorphous silicon layer 107 and oxide layer 108, forms a substantially orthogonal angle with the lower conductive terminal 101 and the upper conductive terminal 131. This "double corner" formation of the composite antifuse layer enhances the electric field at this location during programming, thereby ensuring a predictable location, and therefore resistance, of filament 132.

Furthermore, the present invention provides advantages under shearing conditions due to stress relaxation in the programmed antifuse. Specifically, stress relaxation typically occurs within a structure, not at its boundaries. Therefore, referring back to Figure 2B, if shearing occurs in prior art antifuse 20, the sheared portion 19' of filament 19 significantly reduces the surface area 19A for conducting current, thereby resulting in instability of the resistance provided by antifuse 20. In contrast, filament 132 of the present invention which is formed at one of the boundaries of antifuse 130 is substantially unaffected by shearing conditions caused by stress relaxation. Therefore, an antifuse in accordance with the present invention provides a low, stable resistance even under the above-described adverse conditions.

Therefore, the antifuse of the present invention provides the following advantages: a predictable location of the antifuse filament, minimal shearing effects on the filament, a relatively low programming voltage, and a low, stable resistance value.

The above description of the present invention is meant to be illustrative only and not limiting. Other embodiments will be apparent to those skilled in the art in light of the detailed description. The present invention is set forth in the appended claims.

CLAIMS

We claim:

1. An antifuse comprising:

a first conductive layer;

an antifuse layer formed on said first conductive layer; and

a second conductive layer formed on said antifuse layer, wherein a portion of said antifuse layer forms a substantially orthogonal angle with said first conductive layer and said second conductive layer.

2. The antifuse of Claim 1 wherein said antifuse layer includes an amorphous silicon layer.

3. The antifuse of Claim 2 wherein said amorphous silicon layer has a thickness between 350Å and 550Å.

4. The antifuse of Claim 3 wherein said amorphous silicon layer has a thickness of approximately 450Å.

5. The antifuse of Claim 2 wherein said antifuse layer further includes a first oxide layer formed between said first conductive layer and said amorphous silicon layer.

6. The antifuse of Claim 5 wherein said first oxide layer is formed from said first conductive layer.

7. The antifuse of Claim 5 wherein said first oxide layer has a thickness between 35Å and 70Å.

8. The antifuse of Claim 5 wherein said first oxide layer is titanium oxide.

9. The antifuse of Claim 5 wherein said first oxide layer is tungsten oxide.

10. The antifuse of Claim 5 wherein said first oxide layer is a combination of titanium oxide and tungsten oxide.

11. The antifuse of Claim 5 wherein said antifuse layer further includes a second oxide layer formed between said amorphous silicon layer and said second conductive layer.

12. The antifuse of Claim 11 wherein said second oxide layer is a silicon dioxide layer.

13. The antifuse of Claim 11 wherein said second oxide layer has a thickness between 10Å and 30Å.

14. The antifuse of Claim 11 wherein said second oxide layer completely insulates said amorphous silicon layer from said second conductive layer.

15. The antifuse of Claim 1 wherein said first conductive layer forms a lower conductive terminal of said antifuse.

16. The antifuse of Claim 15 wherein said first conductive layer includes a conductive metal.

17. The antifuse of Claim 16 wherein said conductive metal includes aluminum.

18. The antifuse of Claim 16 wherein said conductive metal includes an aluminum-silicon alloy.

19. The antifuse of Claim 16 wherein said conductive metal includes an aluminum-silicon-copper alloy.

20. The antifuse of Claim 16 wherein said conductive metal includes titanium.

21. The antifuse of Claim 16 wherein said conductive metal includes titanium nitride.

22. The antifuse of Claim 16 wherein said conductive metal includes titanium tungsten.

23. The antifuse of Claim 1 wherein said second conductive layer forms an upper conductive terminal of said antifuse.

24. A method of forming an antifuse comprising the steps of:

forming a first conductive layer on a substrate;

forming an antifuse layer on said first conductive layer; and

forming a second conductive layer on said antifuse layer, wherein said antifuse layer forms a substantially orthogonal angle with each of said first conductive layer and said second conductive layer.

AMENDED CLAIMS

[received by the International Bureau on 22 March 1995(22.03.95); original claims 1 and 5 amended; remaining claims unchanged (2 pages)]

We claim:

1. An antifuse comprising:

a first conductive layer;

a field oxide layer formed on said first conductive layer and having a via formed therein to the top surface of said first conductive layer, wherein said via includes a lower portion forming a profile perpendicular to said first conductive layer, and an upper portion forming a concave profile;

an antifuse layer formed on said first conductive layer, wherein the top surface of said antifuse layer follows the contours of said lower and upper portions of said via; and

a second conductive layer formed on said antifuse layer.

2. The antifuse of Claim 1 wherein said antifuse layer includes an amorphous silicon layer.

3. The antifuse of Claim 2 wherein said amorphous silicon layer has a thickness between 350Å and 550Å.

4. The antifuse of Claim 3 wherein said amorphous silicon layer has a thickness of approximately 450Å.

5. The antifuse of Claim 2 wherein said antifuse layer further includes a first oxide layer formed on the bottom of said via between said first conductive layer and said amorphous silicon layer.

6. The antifuse of Claim 5 wherein said first oxide layer is formed from said first conductive layer.

7. The antifuse of Claim 5 wherein said first oxide layer has a thickness between 35Å and 70Å.

8. The antifuse of Claim 5 wherein said first oxide layer is titanium oxide.

9. The antifuse of Claim 5 wherein said first oxide layer is tungsten oxide.

10. The antifuse of Claim 5 wherein said first oxide layer is a combination of titanium oxide and tungsten oxide.

11. The antifuse of Claim 5 wherein said antifuse layer further includes a second oxide layer formed between said amorphous silicon layer and said second conductive layer.

12. The antifuse of Claim 11 wherein said second oxide layer is a silicon dioxide layer.

13. The antifuse of Claim 11 wherein said second oxide layer has a thickness between 10Å and 30Å.

14. The antifuse of Claim 11 wherein said second oxide layer completely insulates said amorphous silicon layer from said second conductive layer.

15. The antifuse of Claim 1 wherein said first conductive layer forms a lower conductive terminal of said antifuse.

16. The antifuse of Claim 15 wherein said first conductive layer includes a conductive metal.

17. The antifuse of Claim 16 wherein said conductive metal includes aluminum.

18. The antifuse of Claim 16 wherein said conductive metal includes an aluminum-silicon alloy.

19. The antifuse of Claim 16 wherein said conductive metal includes an aluminum-silicon-copper alloy.

20. The antifuse of Claim 16 wherein said conductive metal includes titanium.

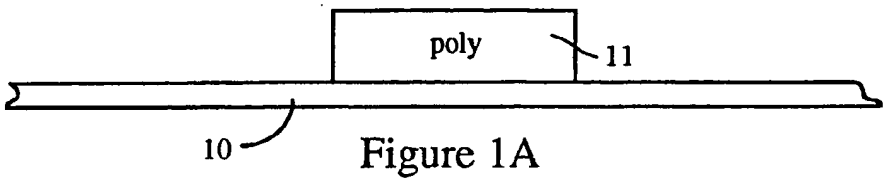


Figure 1A

PRIOR ART

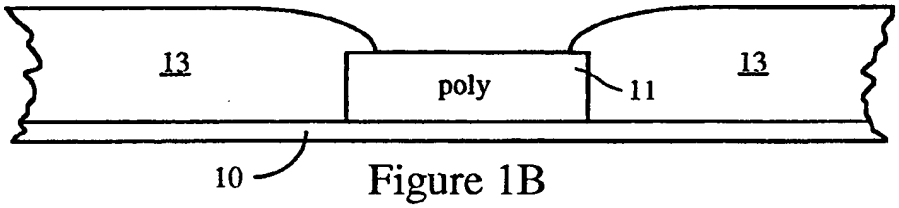


Figure 1B

PRIOR ART

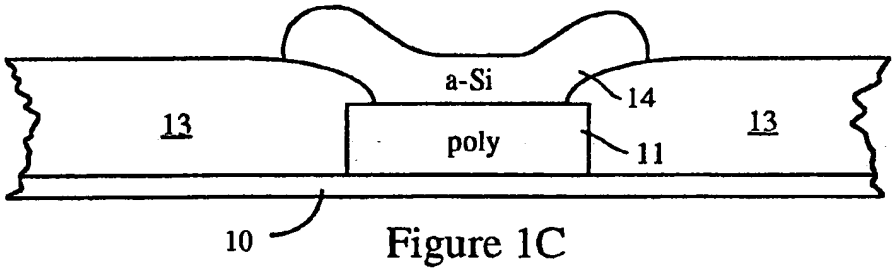


Figure 1C

PRIOR ART

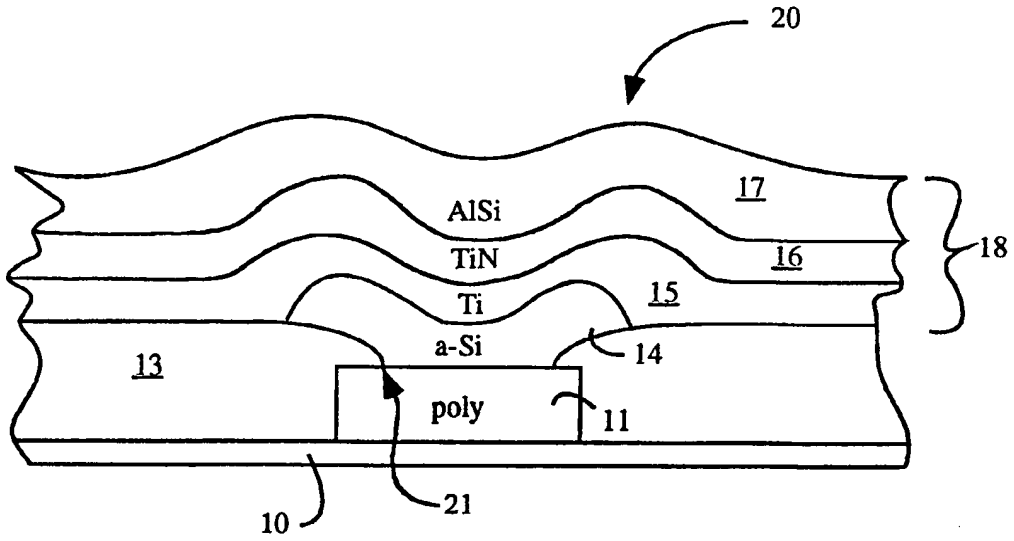


Figure 1D
PRIOR ART

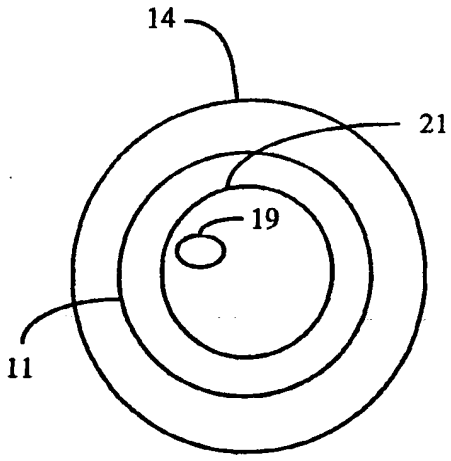


Figure 2A
PRIOR ART

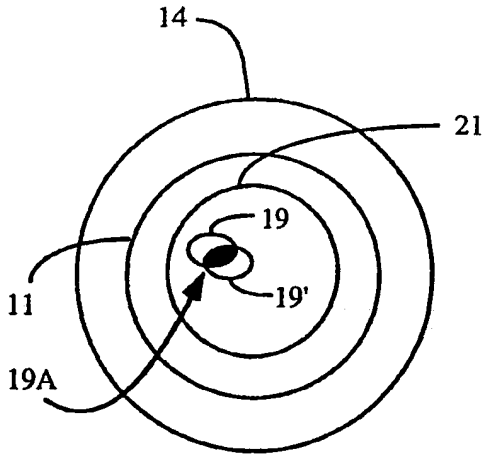


Figure 2B
PRIOR ART

Figure 3A

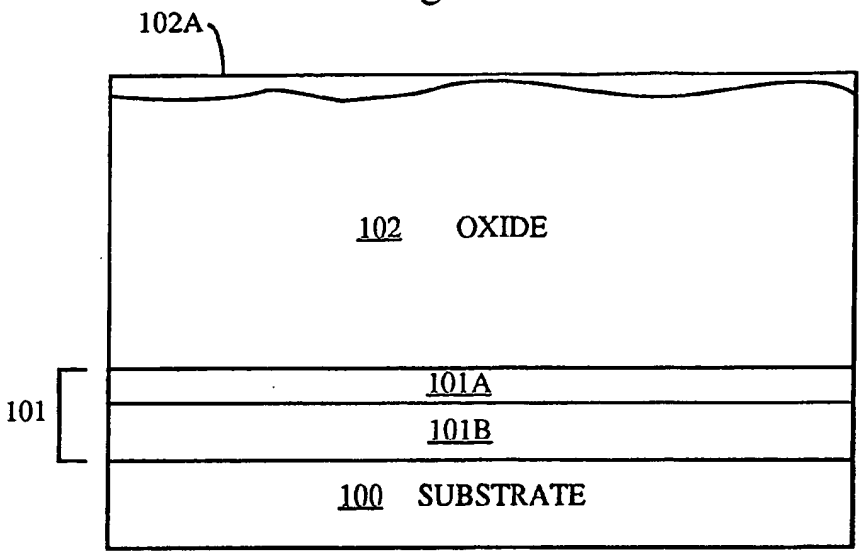


Figure 3B

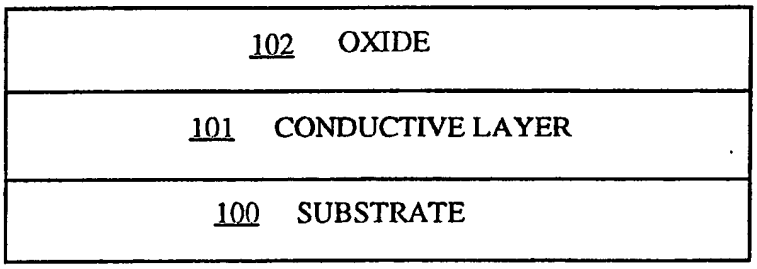


Figure 3C

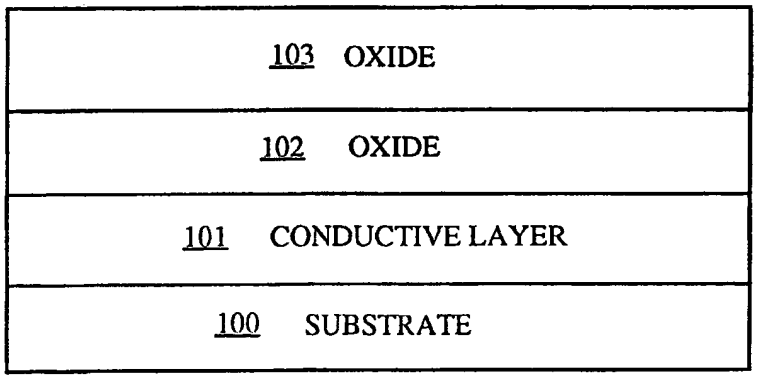


Figure 3D

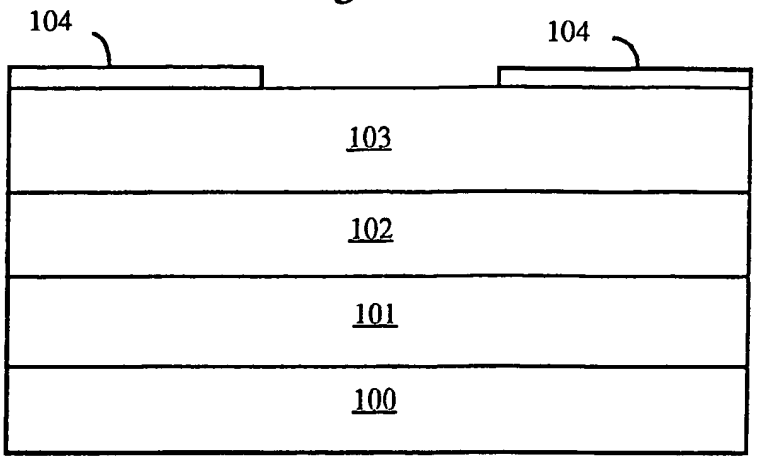


Figure 3E

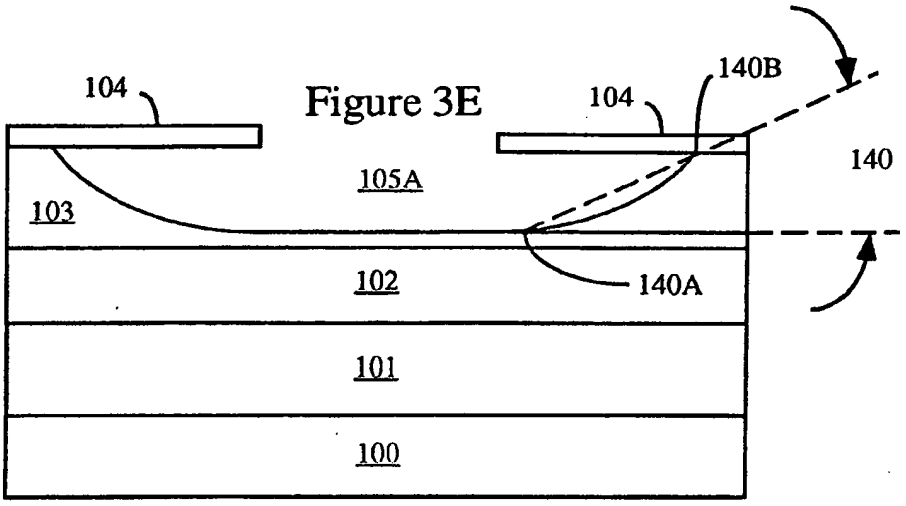


Figure 3F

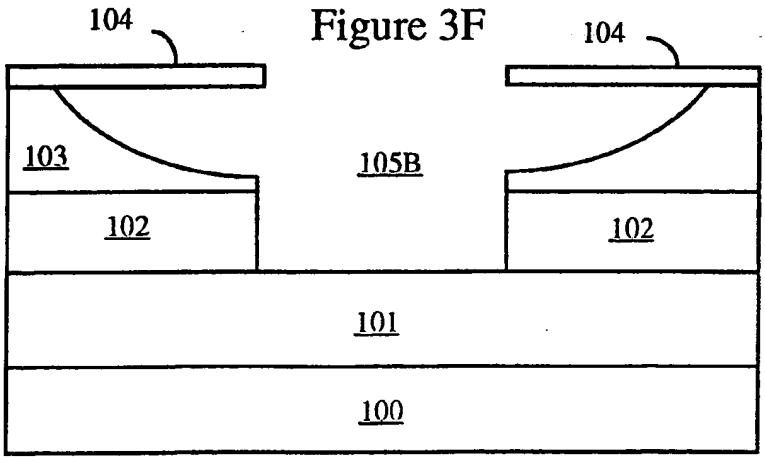


Figure 3G

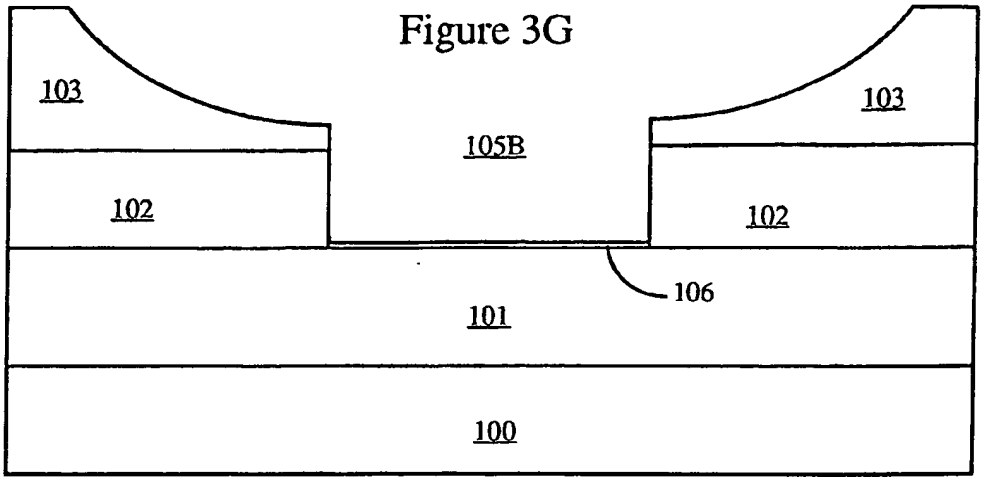


Figure 3H

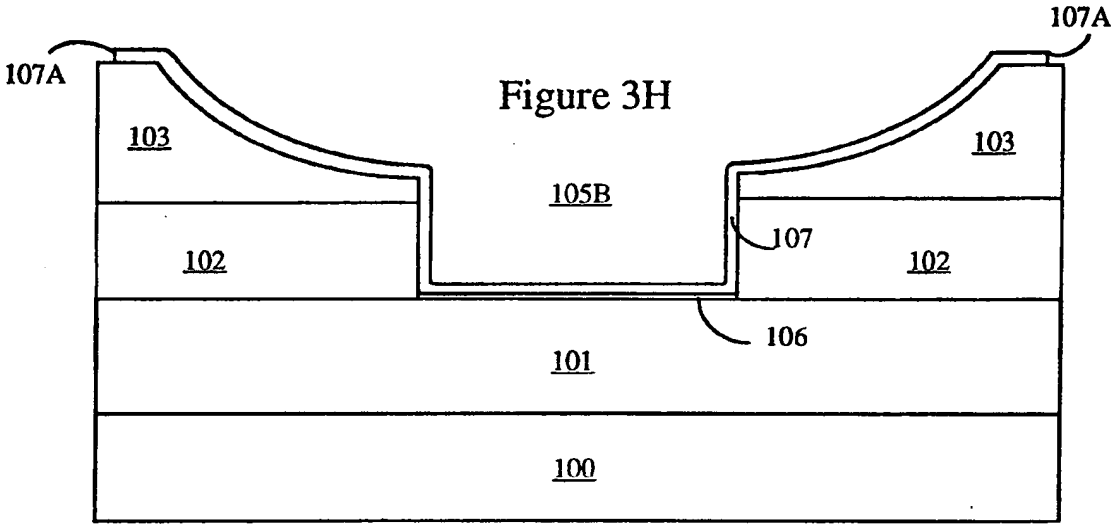
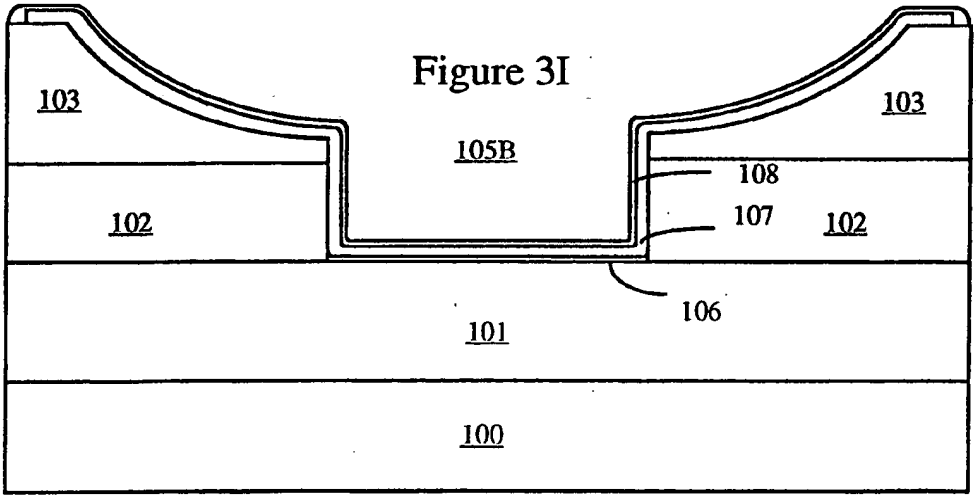


Figure 3I



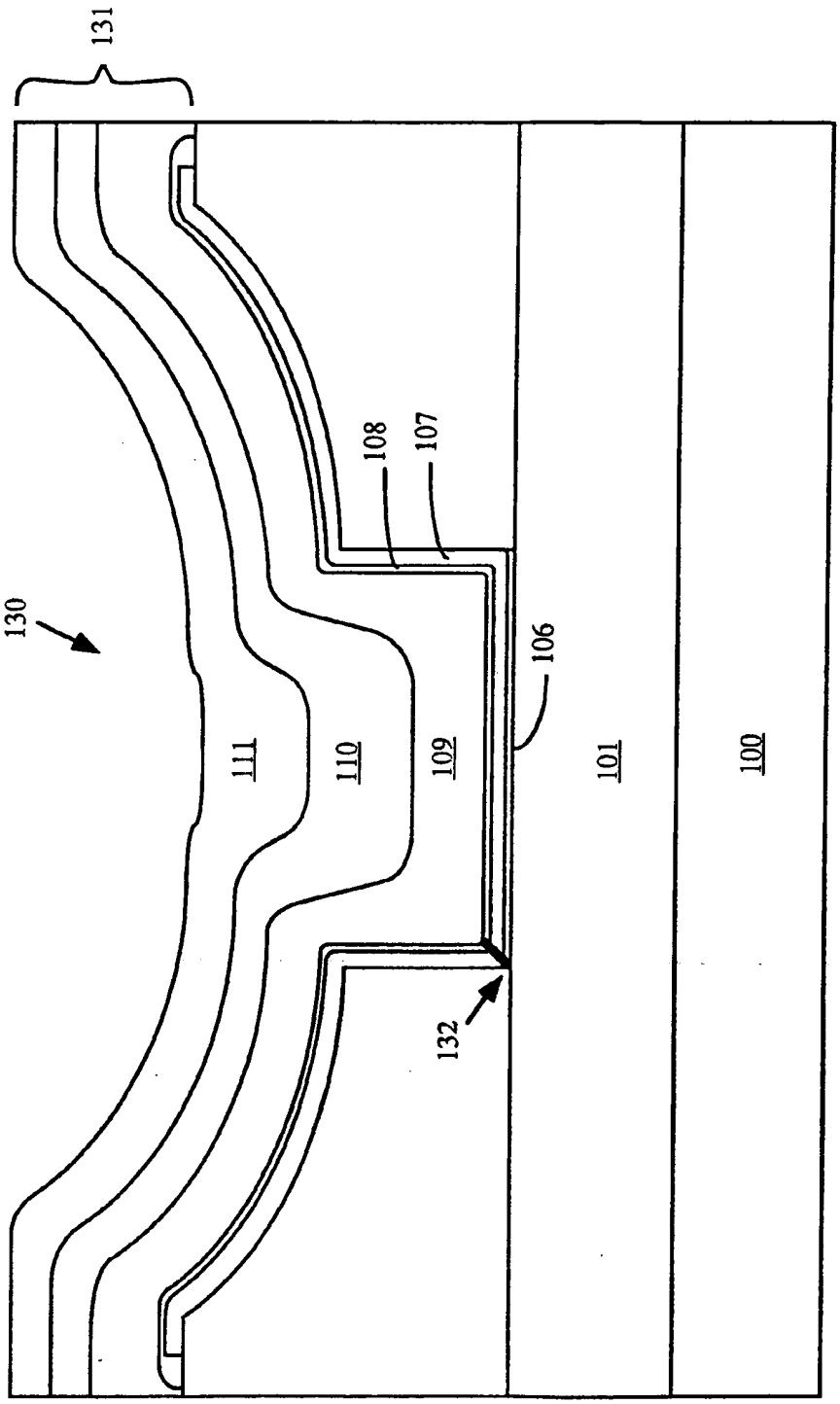


Figure 3J

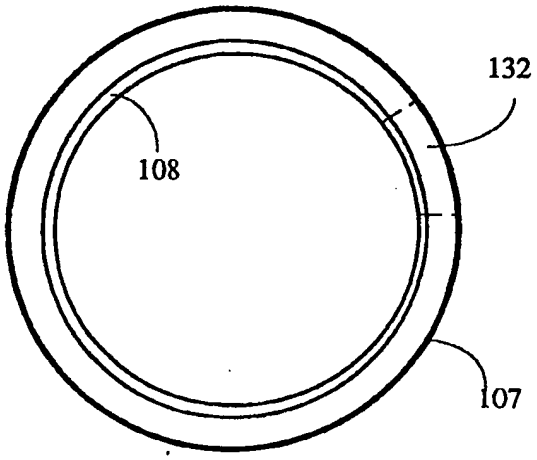


Figure 4

Interr ial Application No
PCT/US 94/11002

A. CLASSIFICATION OF SUB MATTER
IPC 6 H01L23/525

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO,A,92 16976 (CROSSPOINT SOLUTIOS INC) 1 October 1992 see page 8, line 27 - page 9, line 9; figure 2	1,2,15, 16,20-24 5,6,8
X	IEEE ELECTRON DEVICE LETTERS, vol.13, no.1, January 1992, NEW YORK US pages 53 - 55 KUEING-LONG CHEN ET AL 'A sublithographic antifuse structure for field-programmable gate array applications' see page 53, right column; figures 1,2	1,15,24
A	WO,A,92 20095 (QUICKLOGIC CORP) 12 November 1992 see page 8, line 15 - page 9, line 19	1

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 January 1995	24. 01. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Greene, S

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Interl ial pplication No
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C.(Continuation) DOCUMENTS SIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropnate, of the relevant passages	Relevant to claim No.
X	EP,A,0 500 034 (TEXAS INSTRUMENTS INC) 26 August 1992 see column 6, line 41 - line 55; figure 3	1,15,24
Y	EP,A,0 452 091 (ACTEL CORP) 16 October 1991 see column 6, line 19 - column 7, line 52	5,6,8
A	EP,A,0 483 958 (ACTEL CORP) 6 May 1992 see column 5, line 16 - line 42 see column 6, line 7 - line 43	5,11

2

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		EP-A-	0593529	27-04-94
		JP-T-	6509442	20-10-94
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